AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

Claims 1-20 (canceled).

21. (original) A non-volatile memory device, comprising:

a substrate;

a gate dielectric layer on the substrate;

a gate on the gate dielectric layer;

two L-shaped trapping layers on sidewalls of the gate and on the substrate;

two conductive spacers on the sidewalls of the gate, separated from the gate and the substrate by the L-shaped trapping layers;

two doped regions in the substrate beside the conductive spacers; and

a word line over the substrate, contacting with the conductive spacers and top of the gate.

22. (original) The non-volatile memory device of claim 21, wherein each L-shaped trapping layer comprises an ONO composite layer.

23. (original) The non-volatile memory device of claim 21, wherein the gate dielectric layer comprises an oxide layer.

24. (original) The non-volatile memory device of claim 21, wherein the word line, the gate and the conductive spacers comprise doped polysilicon.

25. (original) A non-volatile memory array, comprising:

a substrate;

a plurality of gate structures arranged in rows and columns, each comprising

a gate dielectric layer on the substrate;

a gate on the gate dielectric layer;

two L-shaped trapping layers on sidewalls of the gate and the substrate; and

two conductive spacers on the sidewalls of the gate, separated from the gate and the substrate by the two L-shaped trapping layers;

a plurality of buried drains, each between two columns of gate structures; and

a plurality of word lines over the substrate, each contacting with the two conductive spacers and top of the gate of each of the gate structures in one row.

26. (original) The non-volatile memory array of claim 25, wherein each L-shaped trapping layer comprises an ONO composite layer.

27. (original) The non-volatile memory array of claim 25, wherein the gate dielectric layer comprises an oxide layer.

28. (original) The non-volatile memory array of claim 25, wherein the word lines, the gates and the conductive spacers comprise doped polysilicon.